REMARKS

Claims 1, 2, 4-8 and 15-18 are pending. The specification is being amended. Claims 3 and 9-14 are being cancelled without prejudice or disclaimer of the subject matter recited therein. Claims 1, 2, 4-8 and 15-18 are being amended. No new matter is being added.

Section 2 of the Office Action states that the reference "2001/038350" of the IDS filed 5/5/05 seems to contain an error. It may be that a leading zero needs to be added, namely: "2001/0038350".

In section 3 of the Office Action, the Examiner has requested that the Applicants include a cross-reference to Related Applications. The cross-reference has now been added.

Claims 1, 2, 4 and 5 are currently rejected under 35 USC § 102(e) as being anticipated by US patent publication No. 2002/0175846 (hereinafter referred to as "the Sakimura application"). Applicants are traversing this rejection.

The application now contains two independent claims, namely Claims 1 and 4. Below, Applicants explain that the Sakimura application does not disclose all of the elements of Claims 1 and 4.

According to page 7, paragraph [0100] to page 8, paragraph [0101], the Sakimura application relates to a multi-bit $\Delta\Sigma$ A/D converter that comprises a first analog adder 1a coupled to a first analog integrator 2a, the first analog integrator 2a being coupled to a first analog multiplier 9a. The first analog multiplier 9a is coupled to a second analog adder 1b, the second analog adder 1b being coupled to a second analog integrator 2b. The second analog integrator 2b is coupled to a second analog multiplier 9b, an n-bit quantizer 4 being coupled to the second analog integrator 2b and a most significant bit extractor 5. The most significant bit extractor 5 is coupled to a third digital adder 10c via a so-called "digital processing port" 20 on a first branch and a pair of serially coupled digital differentiators 12a, 12b on a second branch. The most significant bit extractor 5 and the digital processing port 20 are coupled to the first and second analog adders 1a, 1b via a first delay element 8a and a one-bit D/A converter 6 on a feedback path.

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The above circuit configuration of the Sakimura application addresses quantisation noise leakage in the analog integrators 2a, 2b.

Claim 1 recites a continuous time sigma delta converter that comprises conversion means having known non-ideal characteristics. The converter of Claim 1 also comprises a compensation circuit having error modelling components arranged to model substantially the non-ideal characteristics of the conversion means. A summation means is also coupled to combine a compensation signal generated by the compensation circuit and an output signal of the conversion means in order to provide a compensated output signal.

The Sakimura application does not teach "a continuous time sigma delta converter" as recited in Claim 1. The Sakimura application discloses, for example in relation to FIG. 5, the first and second analog integrators 2a, 2b operating in the z-domain, operation in the z-domain being indicative that the conversion means of FIG. 5 is discrete time in nature. Therefore, the Sakimura application discloses a discrete time sigma delta modulator, which is not the same as the continuous time sigma delta converter.

In view of the reasoning provided above, Applicants submit that the Sakimura application dos not anticipate Claim 1.

Claims 2 and 5-8 depend from Claim 1. By virtue of this dependence, Claims 2 and 5-8 are also novel over the Sakimura application.

Claim 4 provides for a method of compensating for known non-ideal characteristics in a continuous time sigma delta converter. As explained above in support of Claim 1, the Sakimura application does not disclose a continuous time sigma delta converter. Accordingly, the Sakimura patent does not anticipate Claim 4.

Claims 15-18 depend from Claim 1. By virtue of this dependence, Claims 15-18 are also novel over the Sakimura application.

Claims 1, 4, 8, 17 and 18 are rejected under 35 USC §102(b) as being anticipated by US Patent No. 6,407,685 (hereinafter referred to as "the Händel patent"). Applicants are traversing this rejection.

As set out above, the application now contains two independent claims, namely claims 1 and 4. Below, Applicants explain that the Händel patent does not disclose all of the elements of Claims 1 and 4.

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The Händel patent relates (col. 8, lines 11-34) to an ADC and an associated calibrator. With particular reference to FIG. 4A, an exemplary ADC 310 and an exemplary calibrator 340 are described in the Händel patent in relation to a receiver 115 of a base station 110. The ADC 310 comprises a sampler 405, a quantizer 410 and a coder 415. The sampler 405 samples an incoming analog signal s(t) and produces a time discrete signal s(k). The time discrete signal is forwarded to the quantizer 410 and then the coder 415 to generate a digital output signal x(k). Thereafter, the calibrator 340 receives the digital output signal x(k) that produces a calibrated digital signal y(k). The calibrator 340 comprises a correction table 350 and calibration logic 320.

The above circuit configuration of the Händel patent serves to provide Nyquist rate ADC calibration using a look-up table (the calibration table 350), i.e. non-linecrities of general ADCs. Hence, the Händel patent is not at all relevant and contrasts with the Sakimura application that is replete with "ΔΣ" references. As explained above, Claim 1 recites a continuous time sigma delta converter that comprises conversion means having known non-ideal characteristics. The converter also comprises the features as previously stated.

The passage of the Händel patent identified by the Examiner does not teach a "sigma delta converter" as recited in Claim 1. The exemplary ADC 310 is simply of a general nature and the passage of the Händel patent identified by the Examiner does not disclose or inherently present sigma deltas.

The Händel patent also does not teach a "continuous time sigma delta converter" as recited in Claim 1. In this respect, processing is performed in the discrete time domain as indicated by the reference at col.8 lines 26-28 to the production of a time discrete signal s(k) by the sampler 405. In view of the reasoning provided above, Applicants submit that the Händel patent does not anticipate Claim 1.

Claim 8 depends from Claim 1. By virtue of this dependence, Claim 8 is also novel over the Händel patent.

Claim 4 provides a method of compensating for known non-ideal characteristics in a continuous time sigma delta converted. As explained above in support of Claim 1, the Händel patent does not disclose a method of compensating for known non-ideal characteristics in a sigma delta converter, but particularly, a method of compensating for known non-ideal characteristics in a continuous time sigma delta converter as recited in Claim 4. Accordingly, the Händel patent does not anticipate Claim 4.

Claims 17 and 18 depend from Claim 1. By virtue of this dependence, Claims 17 and 18 are also novel over the Händel patent.

The case is believed to be in condition for allowance and notice to such effect is respectfully requested. If there is any issue that may be resolved, the Examiner is respectfully requested to telephone the undersigned.

Respectfully submitted,

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